8M x 8bit CMOS Dynamic RAM with Extended Data Out

DESCRIPTION

This is a family of 8,388,608 x 8 bit Extended Data Out Mode CMOS DRAMs. Extended Data Out Mode offers high speed random access of memory cells within the same row. Refresh cycle(4K Ref. or 8K Ref.), access time (-45, -50 or -60), power consumption(Normal or Low power) are optional features of this family. All of this family have CAS-before-RAS refresh, RAS-only refresh and Hidden refresh capabilities. Furthermore, Self-refresh operation is available in L-version. This 8Mx8 EDO Mode DRAM family is fabricated using Samsung′s advanced CMOS process to realize high band-width, low power consumption and high reliability.

FEATURES

- **Part Identification**
  - K4E660812C-JC/L(3.3V, 8K Ref.)
  - K4E640812C-JC/L(3.3V, 4K Ref.)
  - K4E660812C-TC/L(3.3V, 8K Ref.)
  - K4E640812C-TC/L(3.3V, 4K Ref.)

- **Active Power Dissipation**

Unit : mW

Speed	8K	4K
-45	324	432
-50	288	396
-60	252	360

- **Refresh Cycles**

Part NO.	Refresh cycle	Refresh time	
		Normal	L-ver
K4E660812C*	8K	64ms	128ms
K4E640812C	4K		

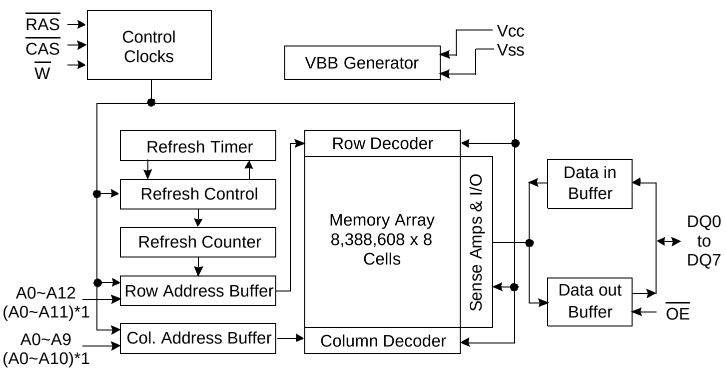
* Access mode & RAS only refresh mode
: 8K cycle/64ms(Normal), 8K cycle/128ms(L-ver.)
CAS-before-RAS & Hidden refresh mode
: 4K cycle/64ms(Normal), 4K cycle/128ms(L-ver.)

- **Performance Range:**

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-45	45ns	12ns	74ns	17ns
-50	50ns	13ns	84ns	20ns
-60	60ns	15ns	104ns	25ns

- Extended Data Out Mode operation
- CAS-before-RAS refresh capability
- RAS-only and Hidden refresh capability
- Self-refresh capability (L-ver only)
- Fast parallel test mode capability
- LVTTL(3.3V) compatible inputs and outputs
- Early Write or output enable controlled write
- JEDEC Standard pinout
- Available in Plastic SOJ and TSOP(II) packages
- +3.3V±0.3V power supply

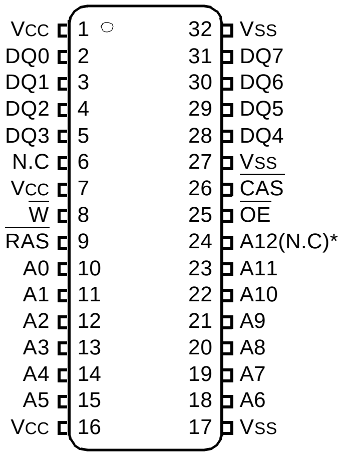
FUNCTIONAL BLOCK DIAGRAM



Note) *1 : 4K Refresh

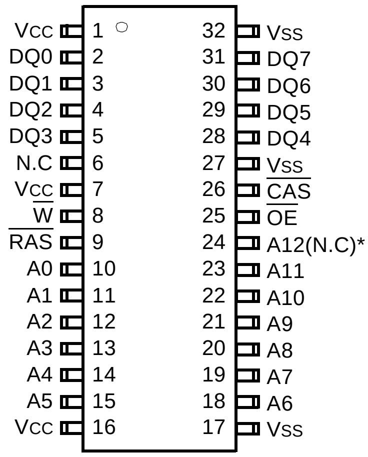
PIN CONFIGURATION (Top Views)

• K4E660812C-J
• K4E640812C-J



(J : 400mil SOJ)

• K4E660812C-T
• K4E640812C-T



(T : 400mil TSOP(II))

* (N.C) : N.C for 4K Refresh product

Pin Name	Pin Function
A0 - A12	Address Inputs(8K Product)
A0 - A11	Address Inputs(4K Product)
DQ0 - 7	Data In/Out
Vss	Ground
RAS	Row Address Strobe
CAS	Column Address Strobe
W	Read/Write Input
OE	Data Output Enable
Vcc	Power(+3.3V)
N.C	No Connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Units
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	Tstg	-55 to +150	°C
Power Dissipation	P_D	1	W
Short Circuit Output Current	I_{OS} Address	50	mA

* Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, T_A= 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0	-	Vcc+0.3*1	V
Input Low Voltage	V_{IL}	-0.3*2	-	0.8	V

*1 : Vcc+1.3V at pulse width≤15ns which is measured at V_{CC}
*2 : -1.3 at pulse width≤15ns which is measured at V_{SS}

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min	Max	Units
Input Leakage Current (Any input $0 \le V_{IN} \le V_{CC}+0.3V$, all other pins not under test=0 Volt)	$I_{I(L)}$	-5	5	uA
Output Leakage Current (Data out is disabled, $0V \le V_{OUT} \le V_{CC}$)	$I_{O(L)}$	-5	5	uA
Output High Voltage Level(I_{OH}=-2mA)	V_{OH}	2.4	-	V
Output Low Voltage Level(I_{OL}=2mA)	V_{OL}	-	0.4	V

DC AND OPERATING CHARACTERISTICS (Continued)

Symbol	Power	Speed	Max		Units
			K4E660812C	K4E640812C	
I_{CC1}	Don't care	-45 -50 -60	90 80 70	120 110 100	mA mA mA
I_{CC2}	Normal L	Don't care	1 1	1 1	mA mA
I_{CC3}	Don't care	-45 -50 -60	90 80 70	120 110 100	mA mA mA
I_{CC4}	Don't care	-45 -50 -60	100 90 80	100 90 80	mA mA mA
I_{CC5}	Normal L	Don't care	0.5 200	0.5 200	mA uA
I_{CC6}	Don't care	-45 -50 -60	120 110 100	120 110 100	mA mA mA
I_{CC7}	L	Don't care	350	350	uA
I_{CCS}	L	Don't care	350	350	uA

I_{CC1}* : Operating Current ($\overline{RAS}$ and $\overline{CAS}$, Address cycling @t_{RC}=min.)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3}* : $\overline{RAS}$-only Refresh Current ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min.)

I_{CC4}* : Extended Data Out Mode Current ($\overline{RAS}$=V_{IL}, $\overline{CAS}$, Address cycling @t_{HPC}=min.)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6}* : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

I_{CC7} : Battery back-up current, Average power supply current, Battery back-up mode
Input high voltage(V_{IH})=V_{CC}-0.2V, Input low voltage(V_{IL})=0.2V, $\overline{CAS}$=$\overline{CAS}$-before-$\overline{RAS}$ cycling or 0.2V
$\overline{W}$, $\overline{OE}$=V_{IH}, Address=Don't care, DQ=Open, T_{RC}=31.25us

I_{CCS} : Self Refresh Current
$\overline{RAS}$=$\overline{CAS}$=0.2V, $\overline{W}$=$\overline{OE}$=A0 ~ A12(A11)=V_{CC}-0.2V or 0.2V, DQ0 ~ DQ7=V_{CC}-0.2V, 0.2V or Open

***Note :** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1}, I_{CC3} and I_{CC6}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A=25°C, V_{CC}=3.3V, f=1MHz)

Parameter	Symbol	Min	Max	Units
Input capacitance [A0 ~ A12]	C_{IN1}	-	5	pF
Input capacitance [$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{W}}$, $\overline{\text{OE}}$]	C_{IN2}	-	7	pF
Output capacitance [DQ0 - DQ7]	C_{DQ}	-	7	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, See note 2)

Test condition : V_{CC}=3.3V±0.3V, Vih/Vil=2.2/0.7V, Voh/Vol=2.0/0.8V

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	74		84		104		ns	
Read-modify-write cycle time	t_{RWC}	101		113		138		ns	
Access time from $\overline{\text{RAS}}$	t_{RAC}		45		50		60	ns	3,4,10
Access time from $\overline{\text{CAS}}$	t_{CAC}		12		13		15	ns	3,4,5
Access time from column address	t_{AA}		23		25		30	ns	3,10
$\overline{\text{CAS}}$ to output in Low-Z	t_{CLZ}	3		3		3		ns	3
Output buffer turn-off delay from $\overline{\text{CAS}}$	t_{CEZ}	3	13	3	13	3	13	ns	6,13
$\overline{\text{OE}}$ to output in Low-Z	t_{OLZ}	3		3		3		ns	3
Transition time (rise and fall)	t_T	1	50	1	50	1	50	ns	2
$\overline{\text{RAS}}$ precharge time	t_{RP}	25		30		40		ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	45	10K	50	10K	60	10K	ns	
$\overline{\text{RAS}}$ hold time	t_{RSH}	8		8		10		ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	35		38		40		ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	7	5K	8	10K	10	10K	ns	14
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	11	33	11	37	14	45	ns	4
$\overline{\text{RAS}}$ to column address delay time	t_{RAD}	9	22	9	25	12	30	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	5		5		5		ns	
Row address set-up time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	7		7		10		ns	
Column address set-up time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	7		7		10		ns	
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	23		25		30		ns	
Read command set-up time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{\text{CAS}}$	t_{RCH}	0		0		0		ns	8
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	0		0		0		ns	8
Write command hold time	t_{WCH}	7		7		10		ns	
Write command pulse width	t_{WP}	6		7		10		ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	8		8		10		ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	7		7		10		ns	
Data set-up time	t_{DS}	0		0		0		ns	9

AC CHARACTERISTICS (Continued)

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Data hold time	t_{DH}	7		7		10		ns	9
Refresh period (Normal)	t_{REF}		64		64		64	ms	
Refresh period (L-ver)	t_{REF}		128		128		128	ms	
Write command set-up time	t_{WCS}	0		0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	24		27		32		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	57		64		77		ns	7
Column address to $\overline{W}$ delay time	t_{AWD}	35		39		47		ns	7
$\overline{CAS}$ set-up time ($\overline{CAS}$ -before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		5		ns	
$\overline{CAS}$ hold time ($\overline{CAS}$ -before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		24		28		35	ns	3
Hyper Page cycle time	t_{HPC}	17		20		25		ns	14
Hyper Page read-modify-write cycle time	t_{HPRWC}	47		47		56		ns	14
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	6.5		7		10		ns	
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	45	200K	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	24		30		35		ns	
$\overline{OE}$ access time	t_{OEA}		12		13		15	ns	3
$\overline{OE}$ to data delay	t_{OED}	8		10		13		ns	
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	36		41		52		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	11	3	13	3	13	ns	6
$\overline{OE}$ command hold time	t_{OEH}	5		5		5		ns	
Write command set-up time (Test mode in)	t_{WTS}	10		10		10		ns	11
Write command hold time (Test mode in)	t_{WTH}	10		10		10		ns	11
$\overline{W}$ to $\overline{RAS}$ precharge time (C-B-R refresh)	t_{WRP}	10		10		10		ns	
$\overline{W}$ to $\overline{RAS}$ hold time (C-B-R refresh)	t_{WRH}	10		10		10		ns	
Output data hold time	t_{DOH}	4		5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	13	3	13	ns	6,13
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	13	3	13	ns	6
$\overline{W}$ to data delay	t_{WED}	8		15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		5		ns	
$\overline{W}$ pulse width (Hyper Page Cycle)	t_{WPE}	5		5		5		ns	
$\overline{RAS}$ pulse width (C-B-R self refresh)	t_{RASS}	100		100		100		us	15,16,17
$\overline{RAS}$ precharge time (C-B-R self refresh)	t_{RPS}	74		90		110		ns	15,16,17
$\overline{CAS}$ hold time (C-B-R self refresh)	t_{CHS}	-50		-50		-50		ns	15,16,17

TEST MODE CYCLE

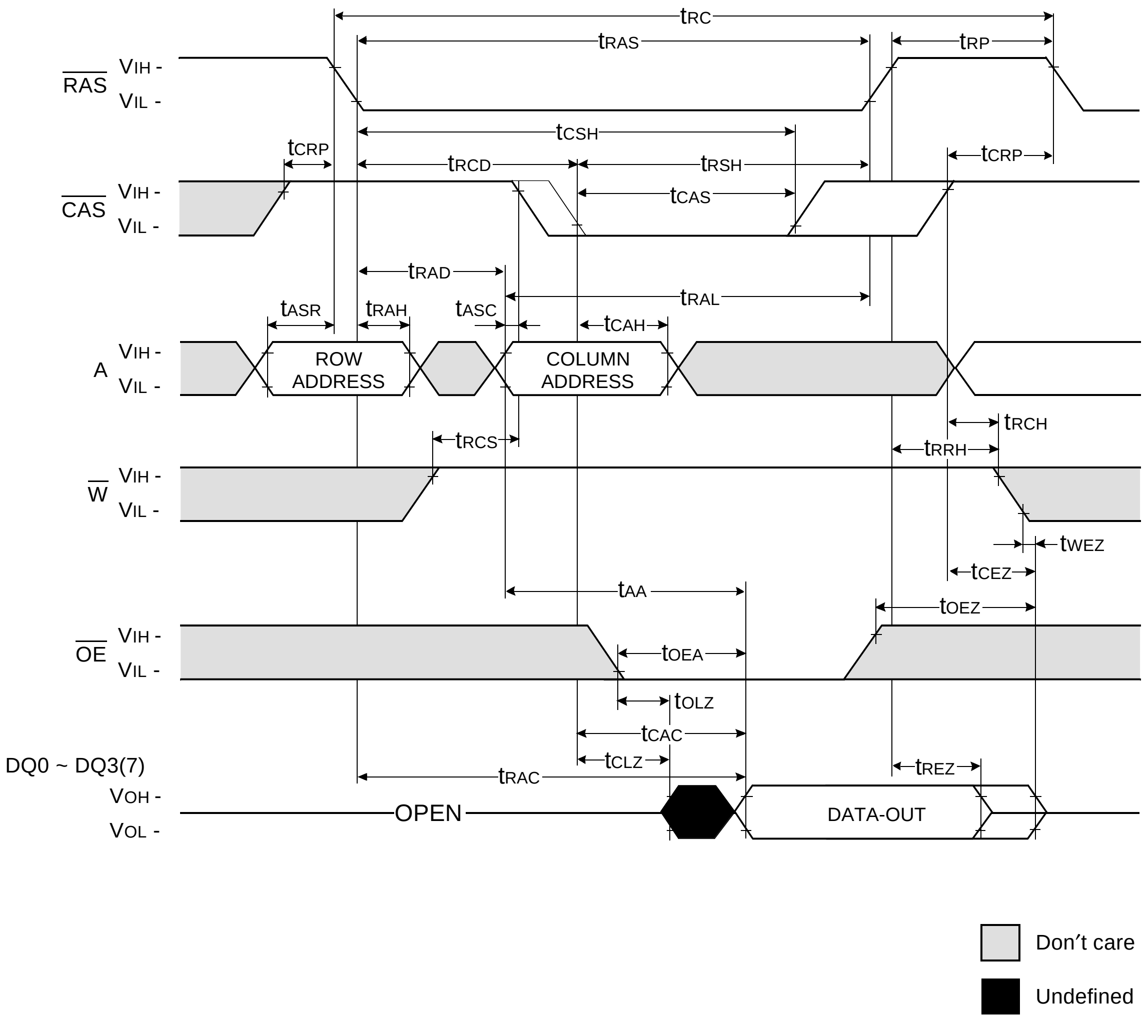
(Note 11)

Parameter	Symbol	-45		-50		-60		Units	Note
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	79		89		109		ns	
Read-modify-write cycle time	t_{RWC}	110		121		145		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		55		65	ns	3,4,10,12
Access time from $\overline{CAS}$	t_{CAC}		17		18		20	ns	3,4,5,12
Access time from column address	t_{AA}		28		30		35	ns	3,10,12
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	55	10K	65	10K	ns	
$\overline{CAS}$ pulse width	t_{CAS}	12	10K	13	10K	15	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	18		18		20		ns	
$\overline{CAS}$ hold time	t_{CSH}	39		43		50		ns	
Column Address to $\overline{RAS}$ lead time	t_{RAL}	28		30		35		ns	
$\overline{CAS}$ to $\overline{W}$ delay time	t_{CWD}	29		35		39		ns	7
$\overline{RAS}$ to $\overline{W}$ delay time	t_{RWD}	62		72		84		ns	7
Column Address to $\overline{W}$ delay time	t_{AWD}	40		47		54		ns	7
Hyper Page cycle time	t_{HPC}	22		25		30		ns	14
Hyper Page read-modify-write cycle time	t_{HPRWC}	52		53		61		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	55	200K	65	200K	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		29		33		40	ns	3
$\overline{OE}$ access time	t_{OEA}		17		18		20	ns	3
$\overline{OE}$ to data delay	t_{OED}	13		18		20		ns	
$\overline{OE}$ command hold time	t_{OEH}	13		18		20		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.
2. Input voltage levels are Vih/Vil. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 2ns for all inputs.
3. Measured with a load equivalent to 1 TTL load and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{oh} or V_{ol}.
7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. This parameters are referenced to the $\overline{CAS}$ falling edge in early write cycles and to the $\overline{W}$ falling edge in $\overline{OE}$ controlled write cycle and read-modify-write cycles.
10. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
11. These specifications are applied in the test mode.
12. In test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} is delayed by 2ns to 5ns for the specified values. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.
13. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going.
    If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
14. $t_{ASC} \geq$6ns, Assume t_T = 2.0ns, if $t_{ASC} \leq$6ns, then t_{HPC}(min) and t_{CAS}(min) must be increased by the value of "6ns-t_{ASC}".
15. If $t_{RASS} \geq$100us, then $\overline{RAS}$ precharge time must use t_{RPS} instead of t_{RP}.
16. For $\overline{RAS}$-only-Refresh and Burst $\overline{CAS}$-before-$\overline{RAS}$ refresh mode, 4096 cycles(4K/8K) of burst refresh must be executed within 64ms before and after self refresh, in order to meet refresh specification.
17. For distributed $\overline{CAS}$-before-$\overline{RAS}$ with 15.6us interval, CBR refresh should be executed with in 15.6us immediately before and after self refresh in order to meet refresh specification.

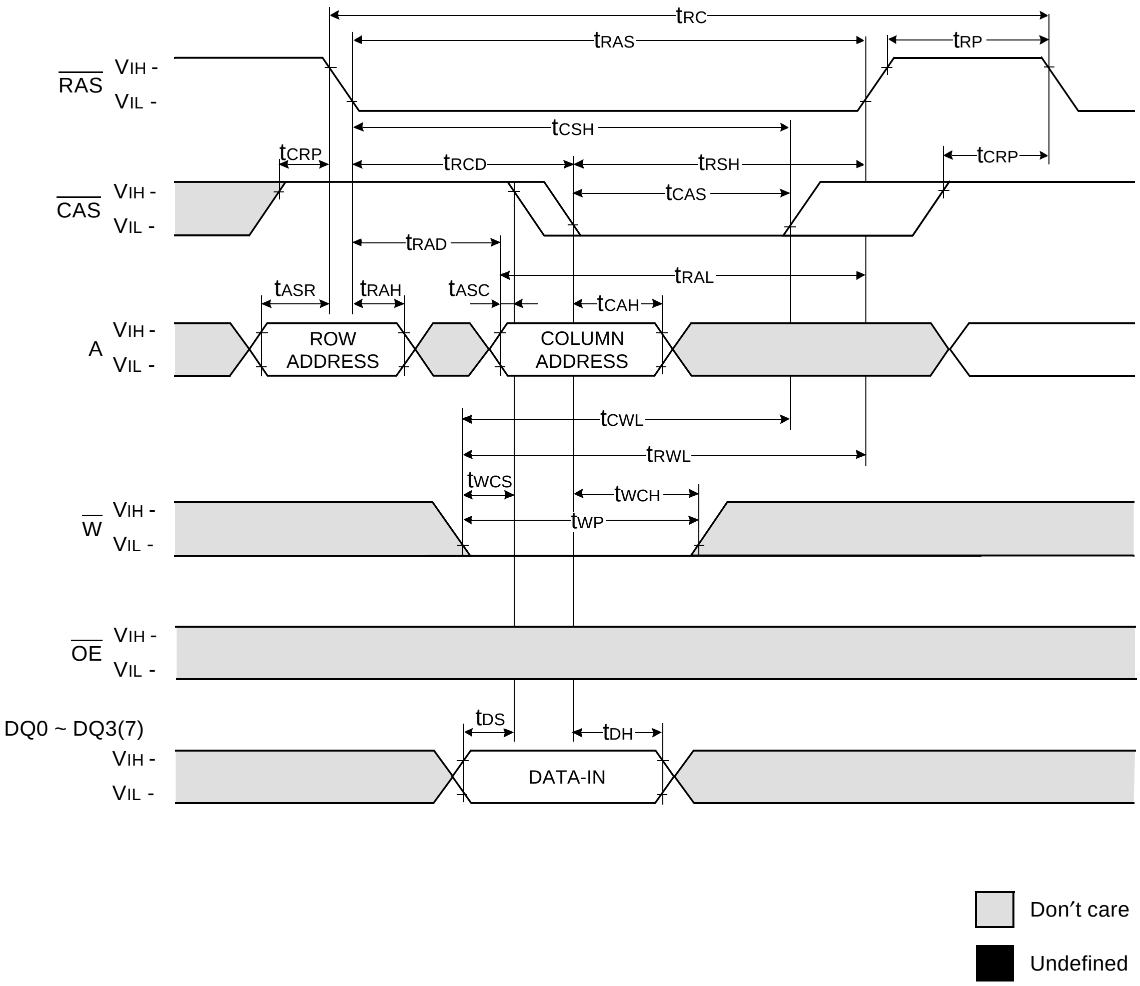
READ CYCLE



tRC
tRAS
tRP
RAS
VIH -
VIL -
tCSH
tCRP
tRCD
tRSH
tCRP
CAS
VIH -
VIL -
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A
VIH -
VIL -
ROW
ADDRESS
COLUMN
ADDRESS
tRCH
tRCS
tRRH
W
VIH -
VIL -
tWEZ
tCEZ
tAA
tOEZ
OE
VIH -
VIL -
tOEA
tOLZ
tCAC
DQ0 ~ DQ3(7)
tCLZ
tREZ
tRAC
VOH -
VOL -
OPEN
DATA-OUT
Don′t care
Undefined

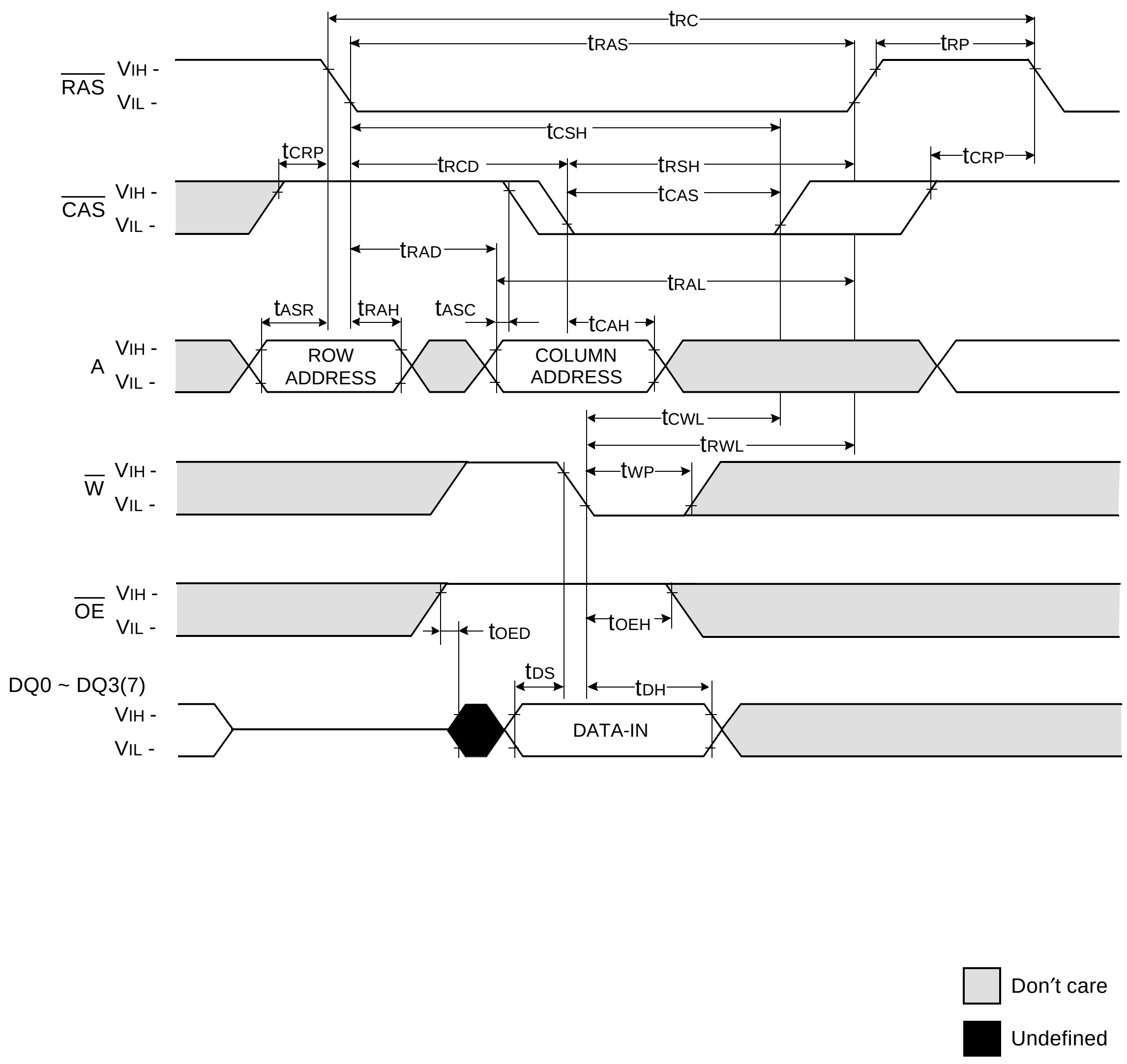
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

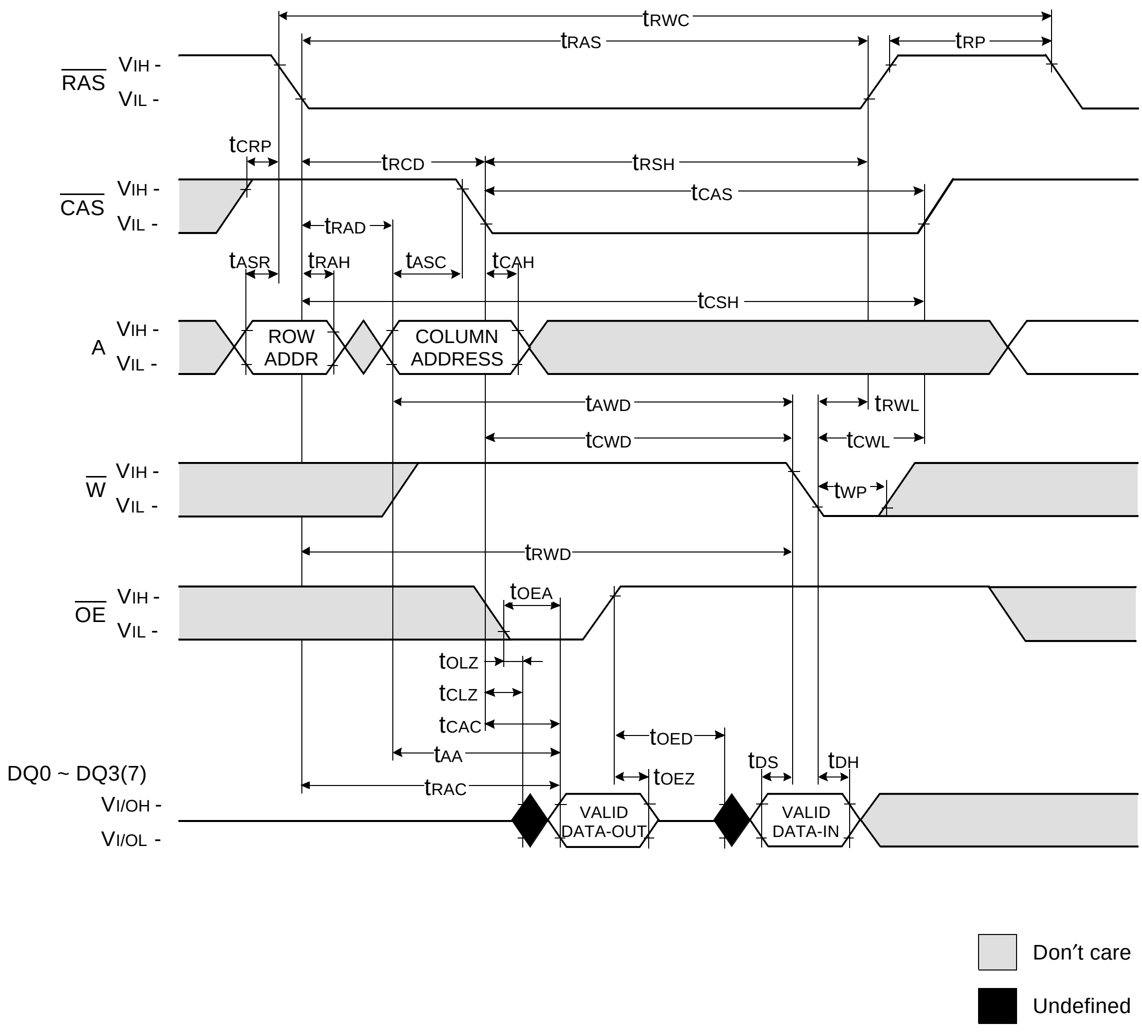


WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

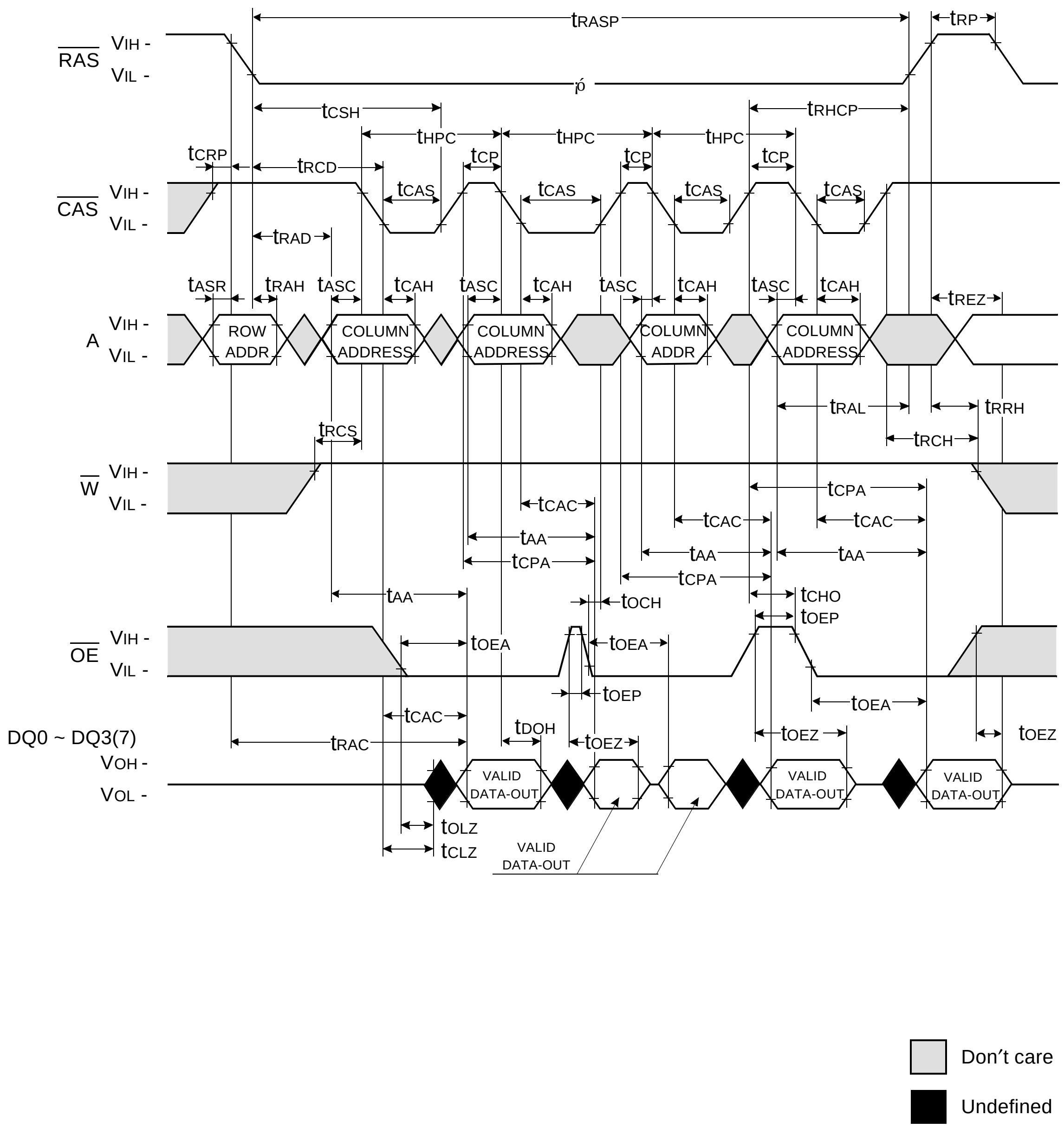
NOTE : DOUT = OPEN



READ - MODIFY - WRITE CYCLE

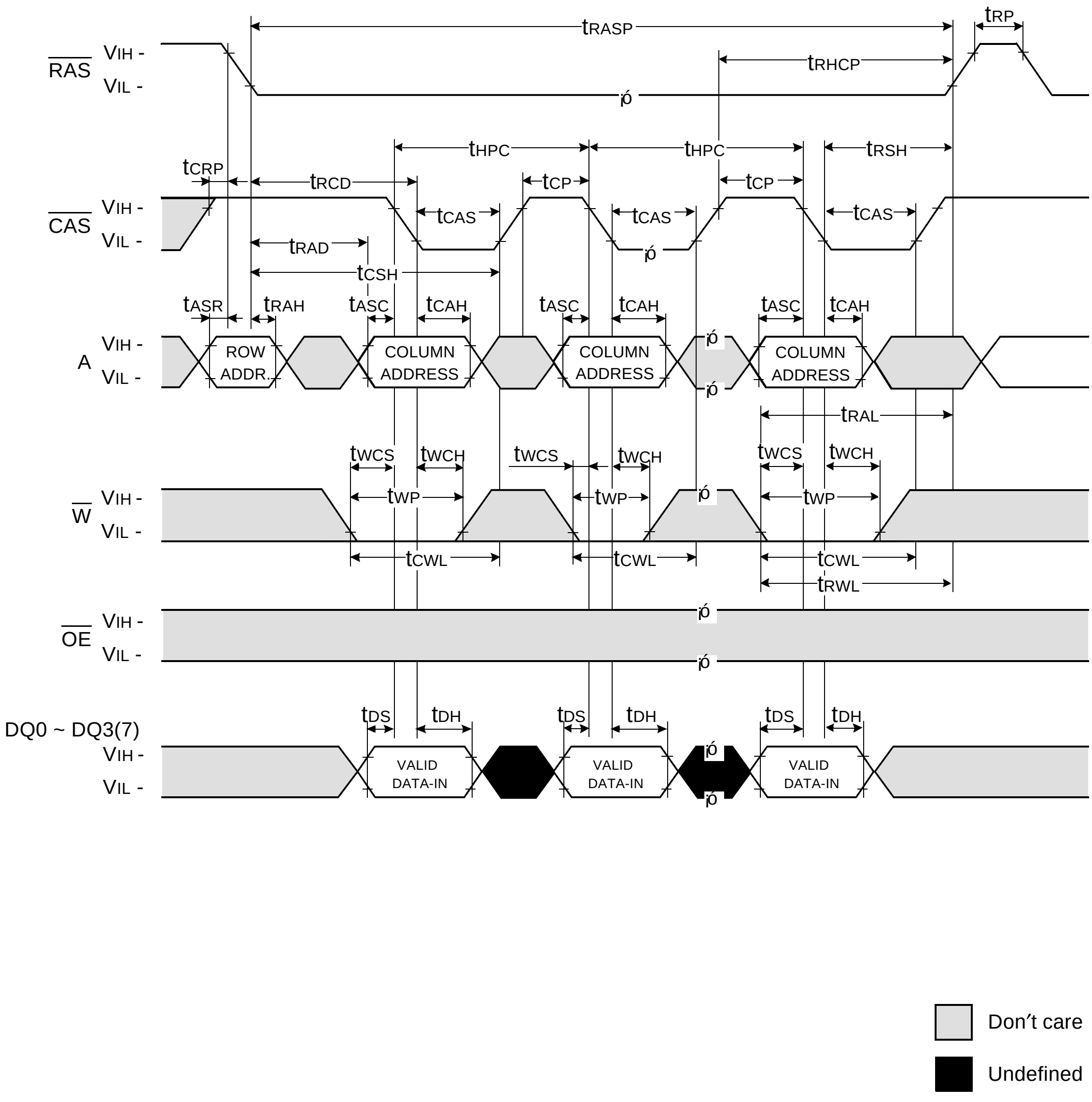


HYPER PAGE READ CYCLE

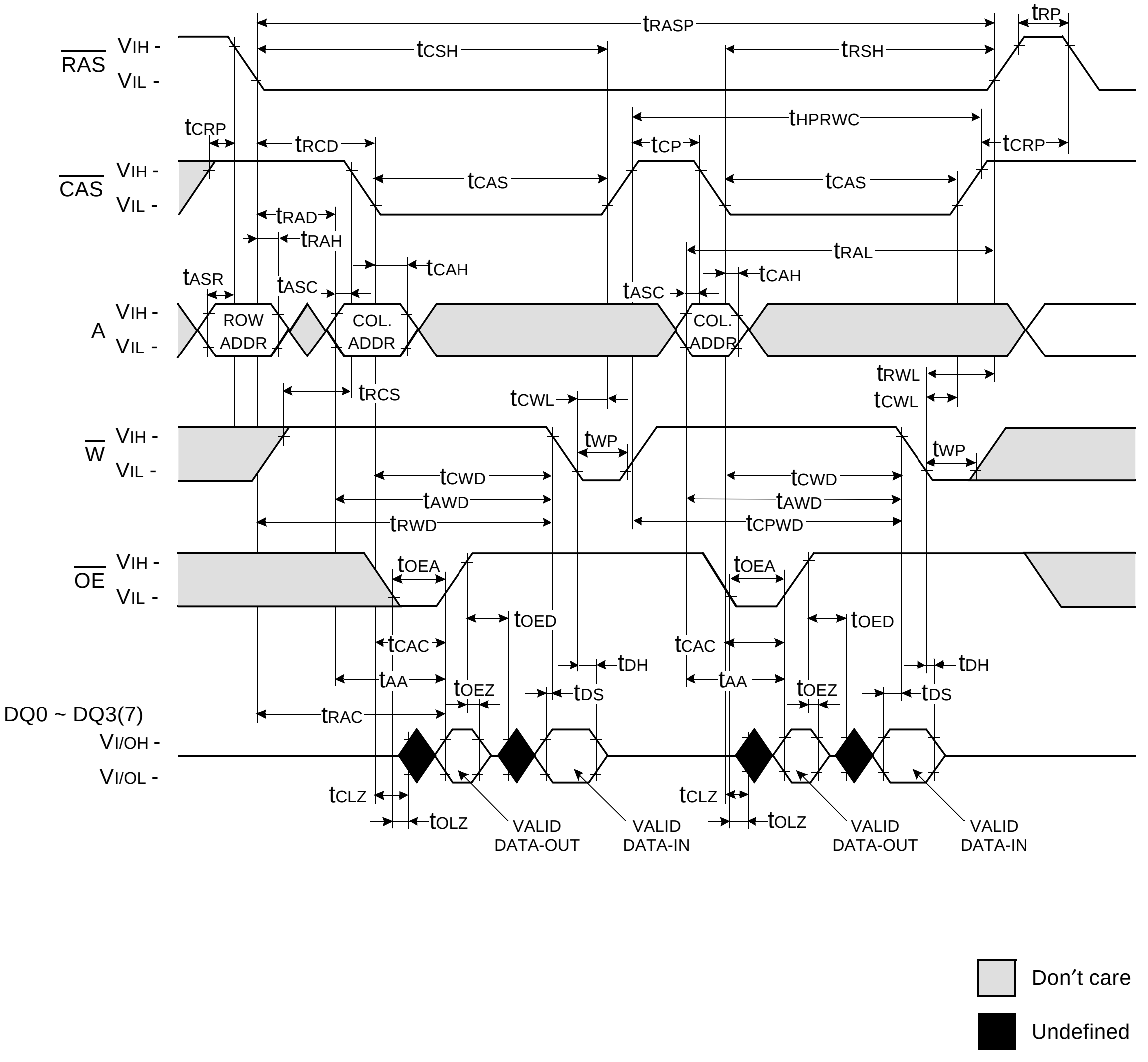


HYPER PAGE WRITE CYCLE (EARLY WRITE)

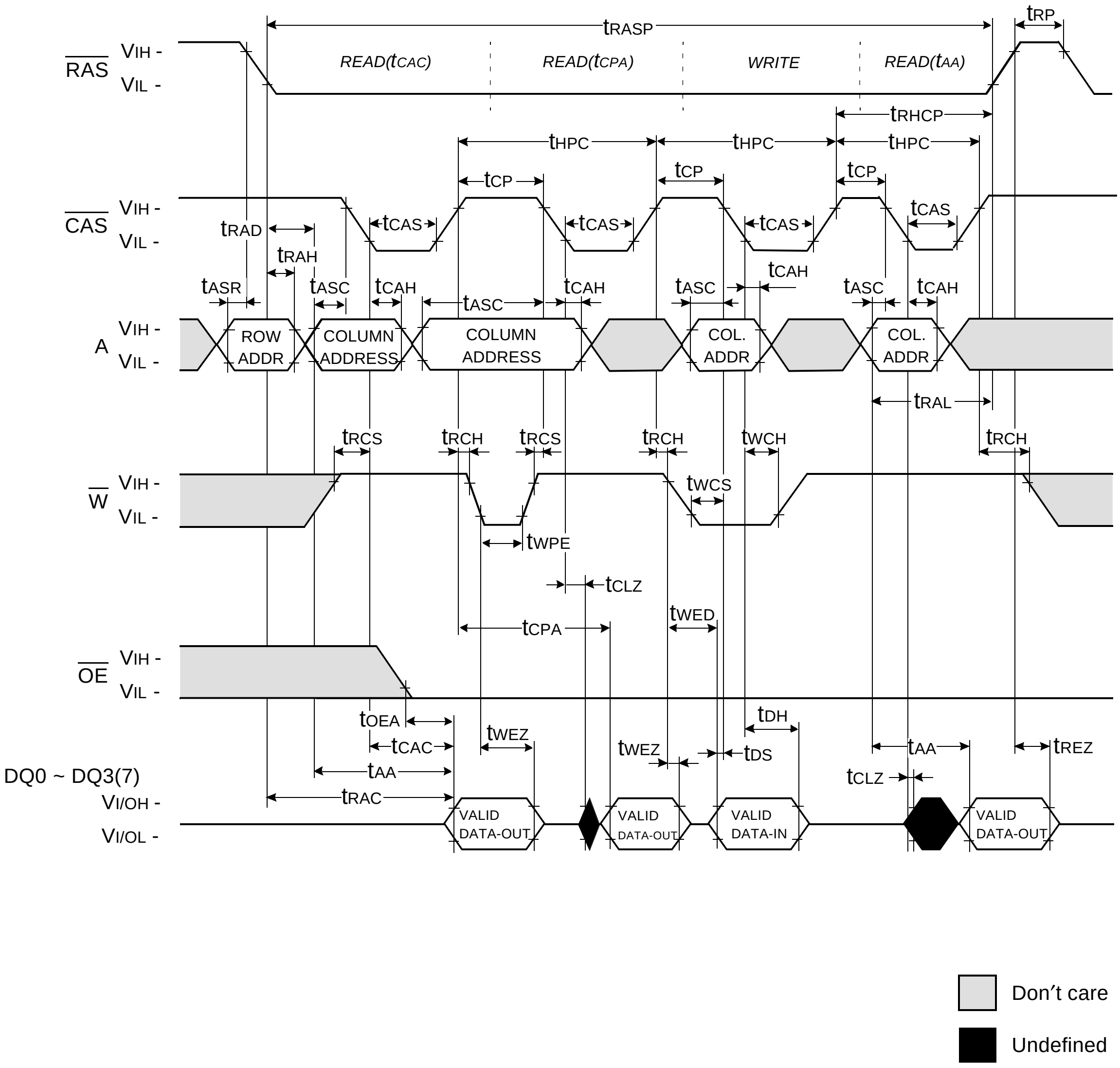
NOTE : DOUT = OPEN



HYPER PAGE READ-MODIFY-WRITE CYCLE



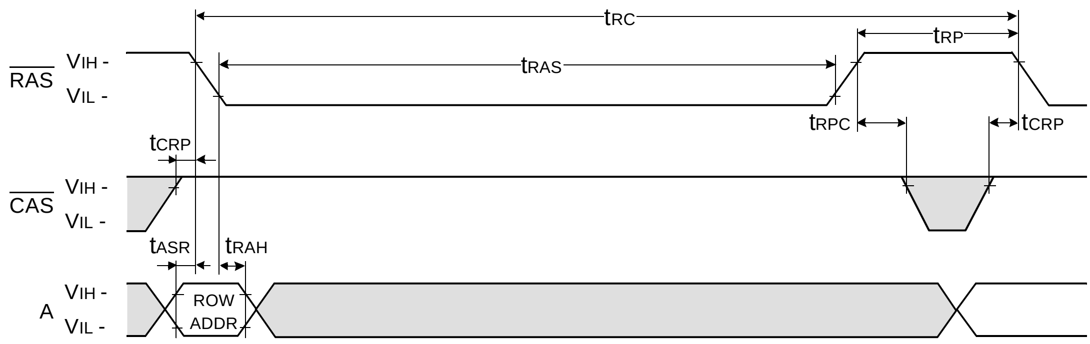
HYPER PAGE READ AND WRITE MIXED CYCLE



RAS - ONLY REFRESH CYCLE*

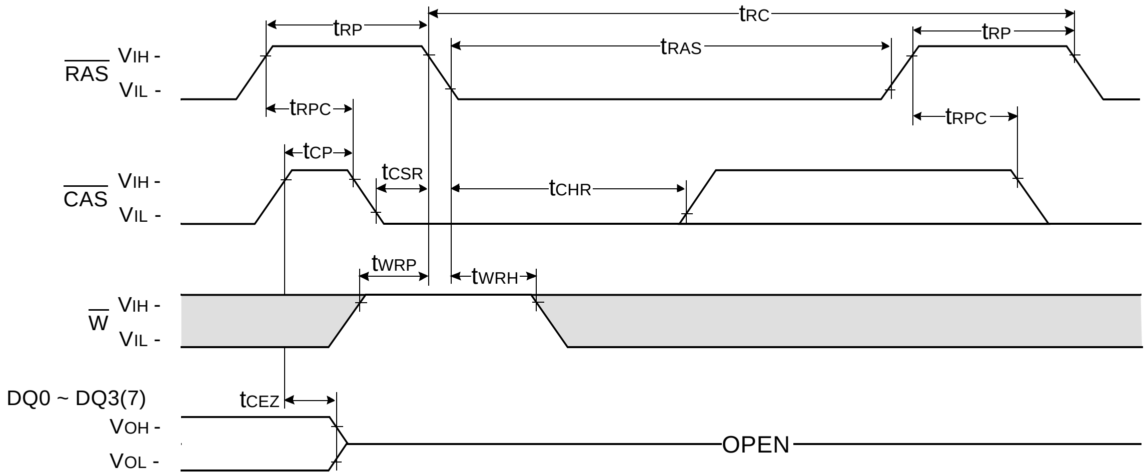
NOTE : W, OE, DIN = Don′t care

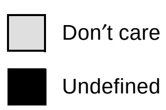
DOUT = OPEN



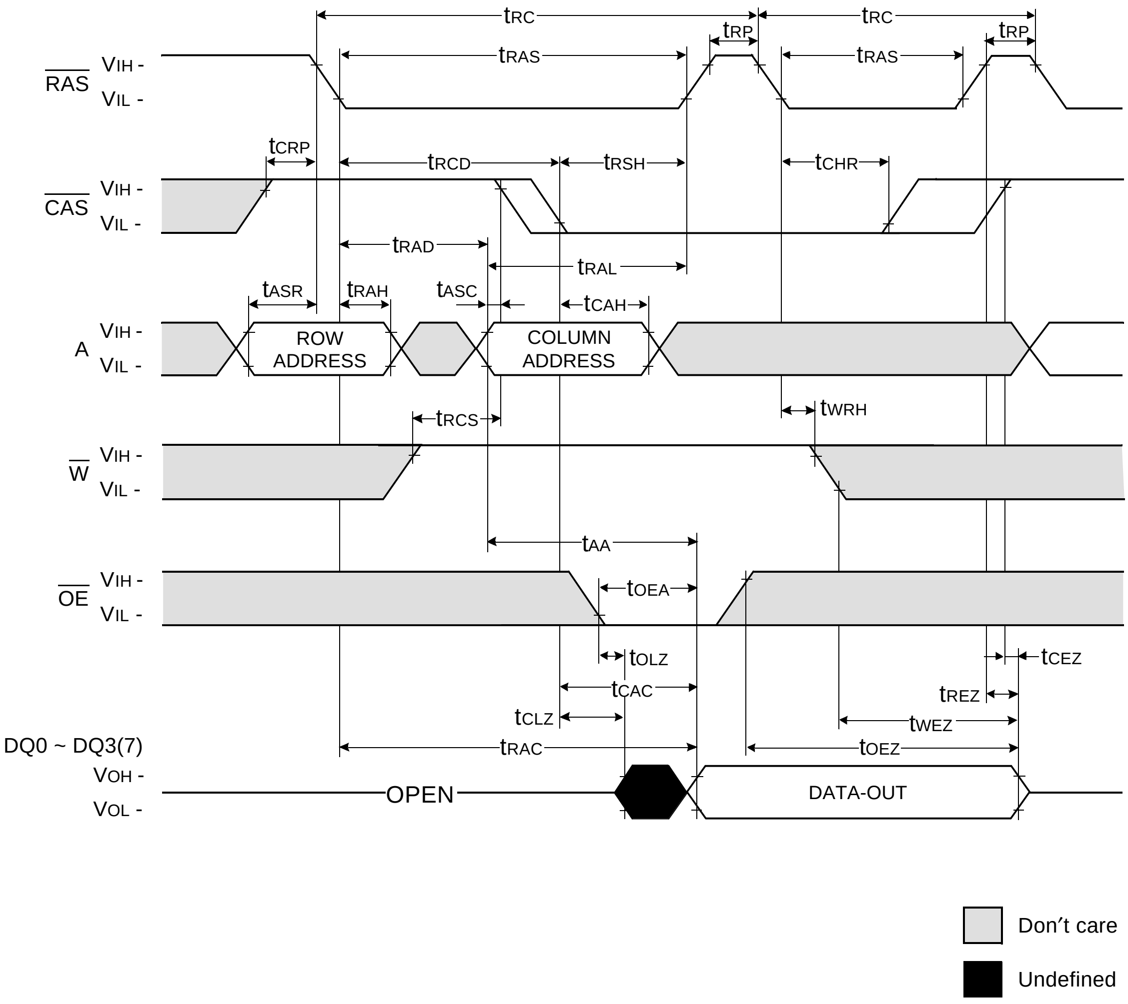
CAS - BEFORE - RAS REFRESH CYCLE

NOTE : OE , A = Don′t care





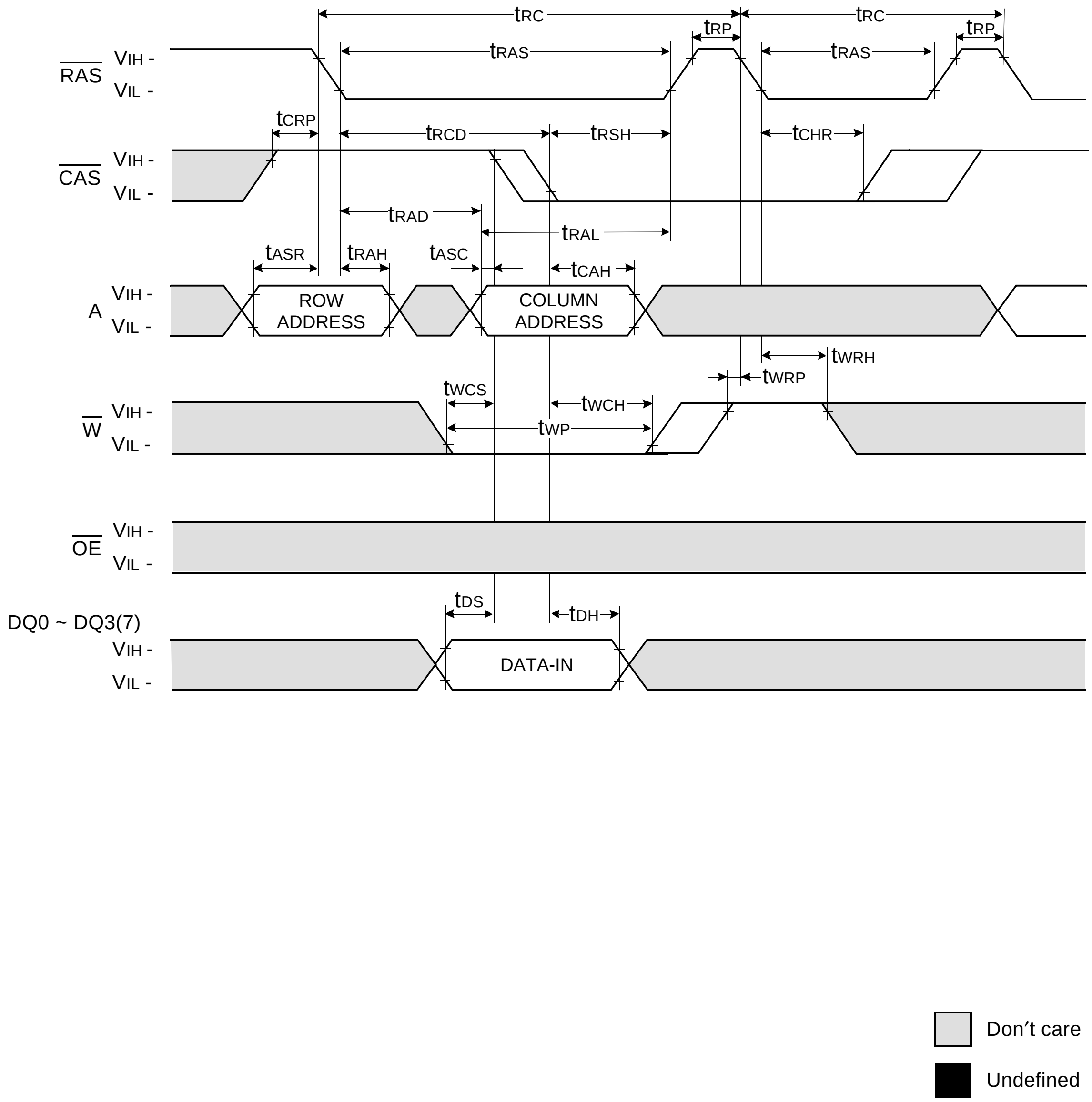
HIDDEN REFRESH CYCLE (READ)



* In Hidden refresh cycle of 64Mb A-dile & B-die, when $\overline{\text{CAS}}$ signal transits from Low to High, the valid data may be cut off.

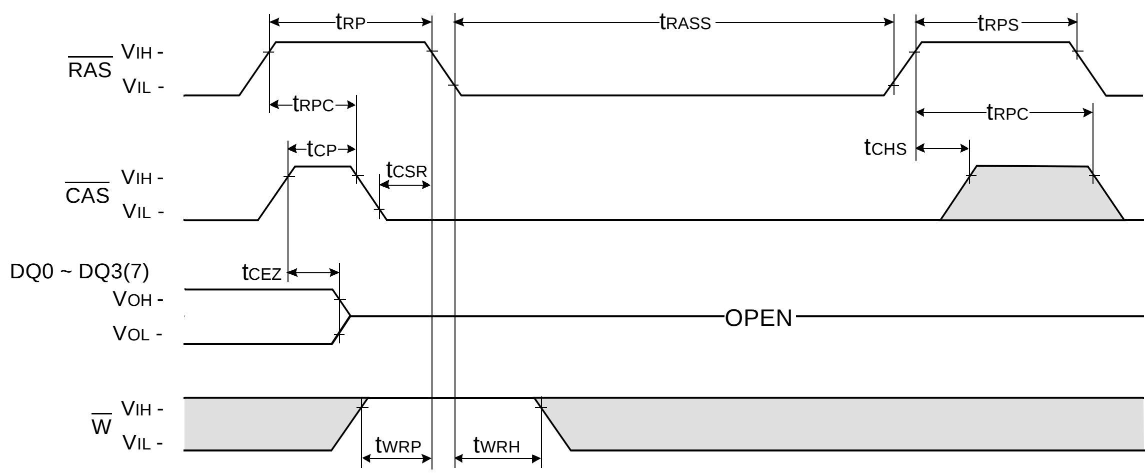
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



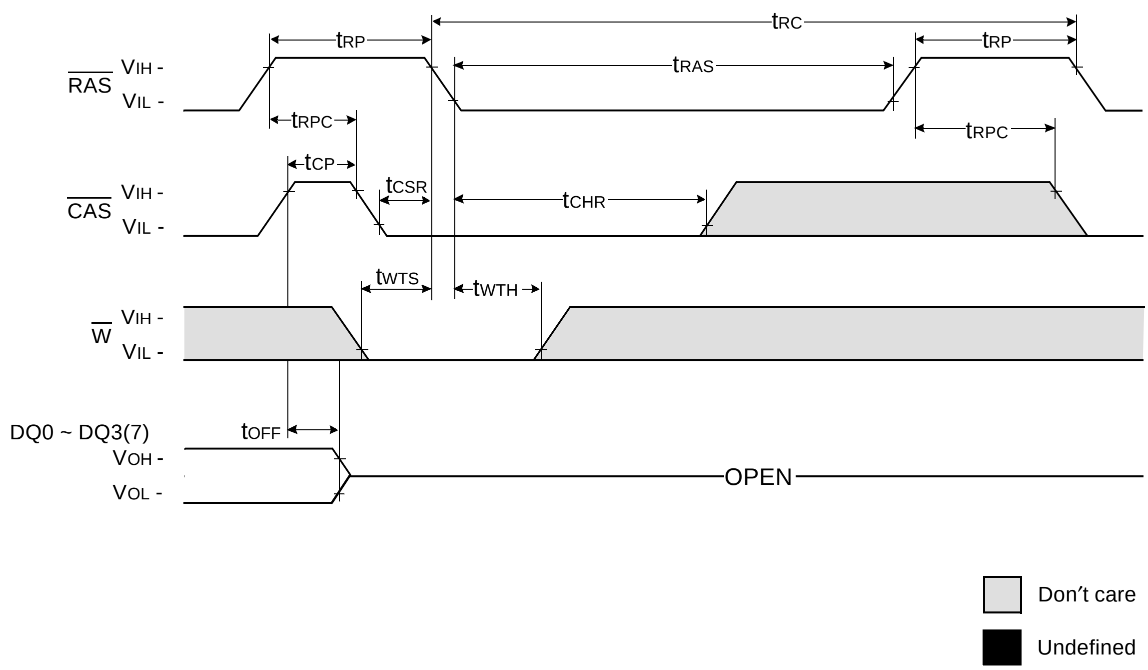
CAS - BEFORE - RAS SELF REFRESH CYCLE

NOTE : OE, A = Don′t care



TEST MODE IN CYCLE

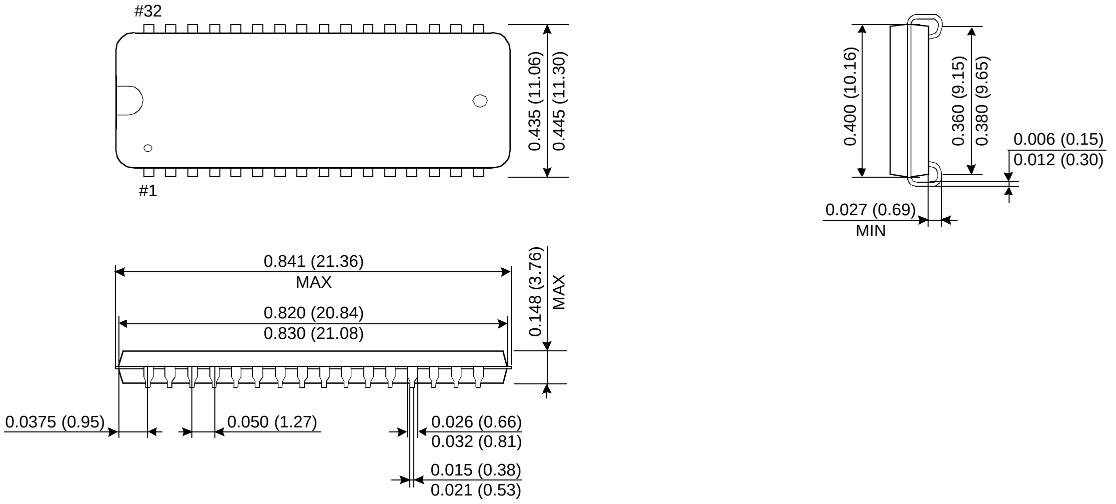
NOTE : OE , A = Don′t care



PACKAGE DIMENSION

32 SOJ 400mil

Units : Inches (millimeters)



32 TSOP(II) 400mil

Units : Inches (millimeters)